WHAT IS CLAIMED IS:

1. A video encoder/decoder coupled to a processor, wherein the video encoder/decoder is configured by the processor a first time to encode/decode data in accordance with a first one of a plurality of data compression/decompression standards.

2. The video encoder/decoder of claim 1, wherein the video encoder/decoder is configured by the processor a second time only if a second one of the plurality of data compression/decompression standards different from the first one of the plurality of data compression/decompression standards is selected for encoding/decoding.

3. The video encoder/decoder of claim 2 wherein the video encoder/decoder is configured by configuring a configuration register disposed within the video encoder/decoder.

4. The video encoder/decoder of claim 3 further comprising a memory which stores the configuration data for each of the plurality of the data compression/decompression standards, wherein the processor reads the configuration data from the memory and loads the same into the configuration register.

5. The video encoder/decoder of Claim 1 further comprising a vector pipeline unit, the vector pipeline unit further comprising:

a run-length decoder which receive data elements of a data vector at its input terminals and decodes and supplies to its output terminals one of the data elements received thereby if the run-length decoder is disabled and a run-length of the data elements received thereby if the run-length decoder is enabled, wherein each data element comprises a plurality of bits.

6. The video encoder/decoder of Claim 5 wherein the run-length decoder is disabled if a bit associated therewith in the configuration register is reset.

7. The video encoder/decoder of Claim 6 wherein the vector pipeline unit further comprises:

an ALU having a plurality of first input terminals which receive the data element supplied thereto by the run-length decoder, a plurality of second input terminals which receive a second data element of the vector and a plurality of output terminals; the ALU to deliver to its output terminals one of a result of a plurality of arithmetic or logic

operations performed thereby if the ALU is enabled and the first data element received at its first input terminals if the ALU is disabled.

8. The video encoder/decoder of Claim 7 wherein the ALU is disabled if a bit associated therewith in the configuration register is reset.

9. The video encoder/decoder of Claim 8, wherein the vector pipeline unit further comprises:

a multiplier/divider having a plurality of first input terminals which receive the data supplied to the output terminals of the ALU, a plurality of second input terminals which receive a third data element of the vector, the multiplier/divider to supply to its output terminals a result of one of a plurality of multiplication/division operations performed thereby if the multiplier/divider is enabled and the data received at its plurality of first input terminals if the multiplier/divider is disabled.

10. The video encoder/decoder of Claim 9 wherein the multiplier/divider is disabled if a bit associated therewith in the configuration register is reset.

11. The video encoder/decoder of Claim 10, wherein the vector pipeline unit further comprises:

a multiplexer having a plurality of first input terminals which receive a fourth data , a plurality of second input terminals which receive the data supplied to the output terminals of multiplier/divider, a third input terminal and a plurality of output terminals, wherein the third input terminal selects and transfers to the multiplexer's output terminals one of the data supplied to the multiplexer by the multiplier/divider and the fourth data.

12. The video encoder/decoder of Claim 11 wherein the multiplexer transfers to its output terminals the data supplied thereto by the multiplier/divider if a bit associated with the multiplexer in the configuration register is reset.

13. The video encoder/decoder of Claim 12, wherein the vector pipeline unit further comprises:

an accumulator having a plurality of first input terminals which receive the data supplied to the multiplexer's output terminals, and a plurality of second input terminals which receive the second data element of the vector, the accumulator to supply to its output

terminals a result of one of a plurality of arithmetic operations performed thereby if the accumulator is enabled and the data received at its plurality of first input terminals if the accumulator is disabled.

14. The video encoder/decoder of Claim 13 wherein the accumulator is disabled if a bit associated therewith in the configuration register is reset.

15. The video encoder/decoder of Claim 14, wherein the vector pipeline unit further comprises:

a barrel shifter having a plurality of first input terminals which receive the data supplied to the output terminals of the accumulator, wherein the barrel shifter right shifts the data it receives at its plurality of first input terminals if the barrel shifter is enabled.

16. The video encoder/decoder of Claim 15 wherein the barrel shifter supplies the data it receives at its plurality of first input terminals if the barrel shifter is disabled.

17. The video encoder/decoder of Claim 16 wherein the barrel shifter is disabled if a bit associated therewith in the configuration register is reset.

18. The video encoder/decoder of Claim 8, wherein the vector pipeline unit further comprises a round logic unit which receives the data supplied thereto by the barrel shifter and rounds the received data to a nearest integer number, wherein the vector pipeline unit further comprises:

a round logic unit which receives the data supplied thereto by the barrel shifter and rounds the received data to a nearest integer number if the round logic is enabled, wherein the round logic unit supplies the rounded data to its output terminals.

19. The video encoder/decoder of Claim 18, wherein the round logic unit delivers to its output terminals the data supplied thereto by the barrel shifter if the round logic unit is disabled.

20. The video encoder/decoder of Claim 19 wherein the round logic unit is disabled if a bit associated therewith in the configuration register is reset.

21. The video encoder/decoder of Claim 20, wherein the vector pipeline unit further comprises:

a modify logic unit which receives the data supplied thereto by the round logic unit and modifies the received data to one of odd and even number if the modify logic unit is enabled, wherein the modify logic unit supplies the modified data to its output terminals.

22. The video encoder/decoder of Claim 21, wherein the modify logic unit delivers to its output terminals the data supplied thereto by the round logic unit if the modify logic unit is disabled.

23. The video encoder/decoder of Claim 22 wherein the modify logic unit is enabled or disabled by varying a bit associated therewith in the configuration register.

24. The video encoder/decoder of Claim 8, wherein the vector pipeline unit further comprises:

a saturate logic unit which receives the data supplied thereto by the modify logic unit, the saturate logic unit to saturate the received data to a saturate high value if the received data is greater than the saturate high value and if the saturate logic unit is enabled, the saturate logic unit to saturate the received data to a saturate low value if the received data is smaller than the saturate low value and if the saturate logic unit is enabled, wherein the saturate logic unit supplies to its output terminals the saturated data.

25. The video encoder/decoder of Claim 24 wherein the saturate logic unit supplies to its output terminals data it receives from the output terminals of the modify logic unit if the saturate logic unit is disabled.

26. The video encoder/decoder of Claim 25 wherein the saturate logic unit is enabled or disabled by varying a bit associated therewith in the configuration register.

27. The video encoder/decoder of Claim 26, wherein the vector pipeline unit further comprises a status register which collects data supplied thereto by the saturate logic unit and supplies the collected data to a processor, if the status register is enabled.

28. The video encoder/decoder of Claim 27 wherein the status register is enabled or disabled by varying a bit associated therewith in the configuration register.

29. The video encoder/decoder of Claim 8, wherein the vector pipeline unit further comprises a run-length encoder which receives and encodes the run-length of the data that is supplied thereto by the saturate logic unit if the run-length encoder is enabled.

30. The video encoder/decoder of Claim 27 wherein the run-length encoder is enabled or disabled by varying a bit associated therewith in the configuration register.

31. A method of encoding/decoding video data, the method comprising the acts of:

coupling a processor to a video encoder/decoder;

configuring the encoder/decoder via the processor a first time to encode/decode data in accordance with a first one of a plurality of data compression/decompression standards; wherein after the video encoder/decoder is configured it encodes/decodes data according to the first compression/decompression standard.

32. The method of Claim 31 further comprising the act of:

configuring the encoder/decoder via the processor a second time only if a second one of the plurality of data compression/decompression standards different from the first one of the plurality of data compression/decompression standards is selected; wherein after the video encoder/decoder is configured the second time it encodes/decodes data according to the second one of the plurality of data compression/decompression standards.

33. The method of Claim 32 further comprising the act of:

configuring the encoder/decoder by configuring a configuration register disposed therein.

34. The method of Claim 33 further comprising the act of:

storing the configuration data for each of the plurality of compression standards in a memory.

35. The method of Claim 34 further comprising the acts of:

reading the configuration data stored in the memory; and

loading the configuration data read from the memory into the configuration register.

36. The method of Claim 34 wherein the act of storing the configuration data for each of the plurality of compression standards in a memory includes the act of storing the configuration data for each of the plurality of compression standards in a memory that is a ROM.